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DESIGN NOTES

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A Two Wire Isolated and Powered 10-Bit Data Acquisition System

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Introduction

For reasons of safety or to eliminate error producing ground loops, it is often necessary to provide electrical isolation between measurement points and the microprocessor. Unfortunately, the isolated side of this measurement system must still be provided with power. One alternative is to power the isolated side of the circuit with batteries. This solution works if power consumption is low, environmental conditions are mild and the batteries are easily accessible. If these conditions are not met a separate isolated supply may be constructed. This can be both difficult and expensive. This design note describes a transformer isolated system in which one small pulse transformer provides both power and a data path.

The circuit of Figure 1 is a 10-bit data acquisition system with 700V of isolation. The circuit takes advantage of the serial architecture of the LTC1092 which allows data and power to be transmitted using only one transformer. A 10-bit conversion can be completed and the data transferred to the microprocessor in 100μs. Using standard ribbon cable the isolated side of this circuit has been remotely located as much as 50 feet from the transformer without affecting circuit performance.

Circuit Description

In Figure 1, a 4μs wide CS pulse clears the 74HC164 shift registers which will hold the D_{OUT} word of the LTC1092. Additionally, the CS signal sends a 15V pulse through the transformer which charges the 1μf capacitor. The CS pulse width must be in the 2-6μs range for the transformer shown, a small Pulse Engineering model. A pulse more than 6μs will saturate the transformer while a pulse width of less than 2μs will not transfer enough energy through the transformer to keep the isolated supply from drooping during the conversion. The CS pulse can be generated with software or hardware. The LT1021-5 produces a regulated 5V at its output once the 1μf capacitor is charged to approximately 7.2V. The LT1021-5 regulated output powers the isolated side of the circuit. Initially several CS pulses may be required to charge the 1μf capacitor to 7.2V. Once charged however, only one CS pulse per cycle is required to keep the isolated supply from drooping as long as the cycle is repeated every 100μs. The 15V CS signal is also attenuated and delayed. This signal is used to reset the clock circuit and begin the conversion of the LTC1092. The delay is required to allow the transformer flyback to die out before transmitting the D_{OUT} word of the LTC1092 across it.

The clock circuit is a simple oscillator that is gated by a combination of the CS signal and the 74HC161 counter so that for each CS signal the clock circuit generates 12 pulses and then is gated off. These 12 pulses are used to perform the A/D conversion and shift the D_{OUT} word of the LTC1092 into the 74HC164 shift registers where the data can be acquired by the microprocessor.

The D_{OUT} serial data of the LTC1092 is encoded with the clock, differentiated and sent across the transformer. The encoding circuitry pulse width modulates the LTC1092 output. The encoding circuitry uses two one shots to combine the data and the clock. For each negative going clock edge a positive pulse is produced at the output of the encoding circuitry. A wide pulse at the output of the encoding circuitry represents a logical 1 and a narrow pulse represents a logical 0 as shown in the timing diagram of Figure 2. The schottky diodes on the output of the 74HC04 capacitor driver are to protect the driver from damage caused by the initial 15V pulse and the resulting flyback.

The differentiated spikes from the transformer are "integrated" by the schmitt inverters and the 74HC74. Again, schottky diodes as well as current limiting resistors are used to protect the gates from transformer excursions beyond the supplies at their inputs. The encoded data is decoded by one half of the 74HC221 which reconstructs the clock. The 74HC164s convert the data to parallel format.

The 10kΩ pull-up resistor forces the output of the LTC1092 high when the A/D is in the high impedance state. When the A/D output becomes active a start bit (logic 0) is clocked out.

When this initial high to low transition is clocked into bit two of the second 74HC164 it triggers the one shot in the second half of the 74HC221 which provides a load data pulse for the microprocessor.

Summary

The LTC1092 with its simple serial interface is ideally suited for this transformer isolation application. It requires only two isolated lines to transmit 10 bits of data. Additionally, during the time when data is not being transmitted, power for the A/D can be sent through these lines. The circuit provides 700V of isolation and can perform a conversion and shift the data in 100μs. The isolated portion of the circuit can be remotely located up to 50 feet away using ordinary ribbon cable. Possible applications for this circuit are PC-based measurement systems, medical instrumentation, automotive or industrial control loops and other areas where ground loops or large common mode voltages are present.

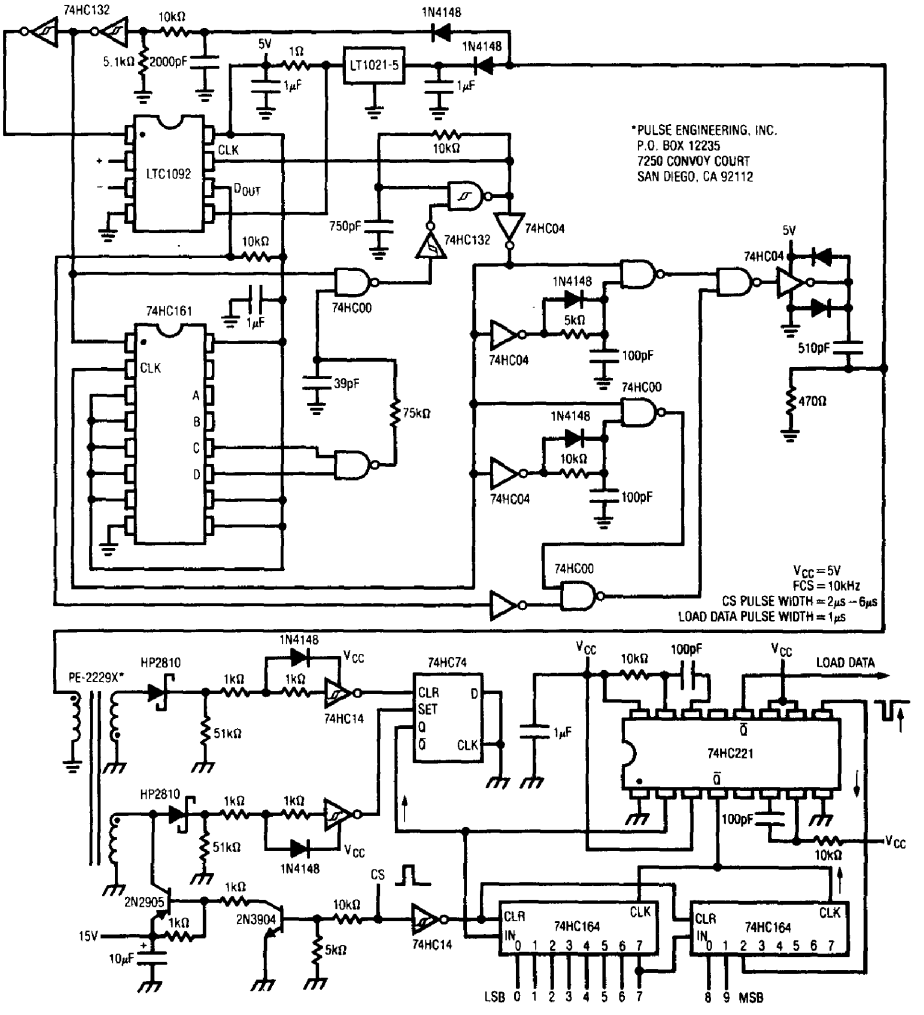

Figure 1. Power and 10-Bit A/D Result Transmitted over Two Isolated Lines

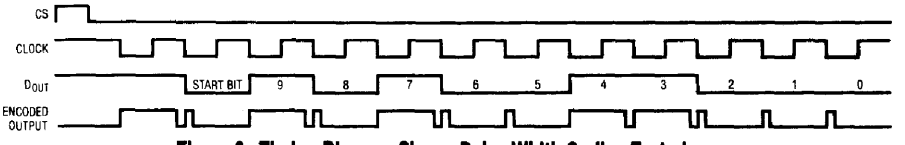

Figure 2. Timing Diagram Shows Pulse Width Coding Technique

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